In the Claims:

Please amend the claims as shown:

Claims 1-117 (Canceled)

Claim 118 (New) An arithmetic method for coding input image data in a predetermined signal format by dividing said image data into block units and by carrying out orthogonal transform in said block units or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding, at a time when output value Y0, i.e., X0 + X1, and output value Y1, i.e., X0-X1, are generated from two input values X0 and X1 by said orthogonal transform or said inverse orthogonal transform, said method comprising:

first, an addition step for adding said X0 to said X1 to generate new X1,

second, a twice value generating step for generating a new X0 being twice the value of said X0, and

third, a subtraction step for subtracting said new X1 from said new X0 to generate newer X0, wherein

said new X1 is used as output value Y0, and said newer X0 is used as output value Y1.

Claim 119. (New) An arithmetic method in accordance with claim 118, wherein said twice value generating step is a multiplying step for multiplying said X0 by 2 to generate said new X0.

Claim 120. (New) An arithmetic method in accordance with claim 118, wherein said twice value generating step is an addition step for adding said X0 to said X0 to generate said new X0.

Claim 121. (New) An arithmetic method in accordance with claim 118, wherein said twice value generating step is a shifting step for shifting said X0 used as a binary number by one bit to a MSB side to generate said new X0.

Claim 122. (New) An arithmetic method for coding input image data in a predetermined signal format by dividing said image data into block units and by carrying out orthogonal transform in said block units or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding at a time when output value Y0, i.e., X0 + X1, and output value Y1, i.e., X0-X1, are generated from two input values X0 and X1 by said orthogonal transform or said inverse orthogonal transform, said method comprising:

first, a subtraction step for subtracting said X1 from said X0 to generate new X0,

second, a twice value generating step for generating new X1 being twice the value of said X1, and

third, an addition step for adding said new X0 to newer X1 to generate new X1, wherein

said newer X1 is used as output value Y0, and said new X0 is used as output value Y1.

Claim 123. (New) An arithmetic method in accordance with claim 122, wherein said twice value generating step is a multiplying step for multiplying said X1 by 2 to generate said new X1.

Claim 124. (New) An arithmetic method in accordance with claim 122, wherein said twice value generating step is an addition step for adding said X1 to said X1 to generate said new X1.

Claim 125. (New) An arithmetic method in accordance with claim 122, wherein said twice value generating step is a shifting step for shifting said X1 used as a binary number by one bit to a MSB side to generate said new X1.

Claim 126. (New) A recording medium including a recorded computer executable program for performing said arithmetic method in accordance with any of claims 118 to 125.

Claim 127. (New) An arithmetic apparatus for coding input image data in a predetermined signal format by dividing said image data into block units and by carrying out orthogonal transform in said block units or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding at a time when output value Y0, i.e., X0 + X1, and output value Y1, i.e., X0 – X1, are generated from two input values X0 and X1 by orthogonal transform or said inverse orthogonal transform, said apparatus comprising:

first, an addition means for adding said X0 to said X1 to generate new X1,

second, a twice value generating means for generating new X0 being twice the value of said X0, and

third, a subtracting means for subtracting said new X1 from said new X0 to generate newer X0, wherein

said new X1 is used as output value Y0, and said newer X0 is used as output value Y1.

Claim 128. (New) An arithmetic apparatus in accordance with claim 127, wherein said twice value generating means is a multiplying means for multiplying said X0 by 2 to generate said new X0.

Claim 129. (New) An arithmetic apparatus in accordance with claim 127, wherein said twice value generating means is an addition means for adding said X0 to said X0 to generate said new X0.

Claim 130. (New) An arithmetic apparatus in accordance with claim 127, wherein said twice value generating means is a shifting means for shifting said X0 used as a binary number by one bit to a MSB side to generate said new X0.

Claim 131. (New) An arithmetic apparatus for coding input image data in a predetermined signal format by dividing said image data into block units and by carrying out orthogonal transform in said block units or for subjecting coded data to inverse orthogonal transform and signal format conversion to obtain image data for decoding at a time when output value Y0, i.e., X0 + X1, and output value Y1, i.e., X0 – X1, are generated from two input values X0 and X1 by said orthogonal transform or said inverse orthogonal transform, said apparatus comprising:

first, a subtraction means for subtracting said X1 from said X0 to generate new X0,

second, a twice value generating means for generating new X1 being twice the value of said X1, and

third, an addition means for adding said new X0 to said new X1 to generate newer X1, wherein

said newer X1 is used as output value Y0, and said new X0 is used as output value Y1.

Claim 132. (New) An arithmetic apparatus in accordance with claim 131, wherein said twice value generating means is a multiplying means for multiplying said X1 by 2 to generate said new X1.

Claim 133. (New) An arithmetic apparatus in accordance with claim 131, wherein said twice value generating means is an addition means for adding said X1 to said X1 to generate said new X1.

Claim 134. (New) An arithmetic apparatus in accordance with claim 131, wherein said twice value generating means is a shifting means for shifting said X1 used as a binary number by one bit to a MSB side to generate said new X1.

REMARKS

Entry and consideration of this Preliminary Amendment are respectfully requested prior to or concurrent with calculation of the filing fees.

The present application is a division of parent application U.S. Application Serial No. 09/380,794, filed September 9, 1999, which is a 371 of PCT/JP98/00969, filed March 10, 1998. Accordingly, a cross-referencing statement has been added to the specification. The Abstract has been amended to conform with the changes made in the parent application. The title has been amended to pertain to the claims pending in this case.

By this Preliminary Amendment, claims 1-117 have been cancelled and claims 118-134 have been added. New claims 118-125 and 127-134 are based upon the original (non-elected) claims from the parent case. Claim 126 is to a recording medium for carrying out the method of claims 118-125.

Applicants respectfully request entry of this Preliminary Amendment.

Respectfully submitted,
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